REMARKS

This is in response to the Office Action dated March 30, 2004. Claims 1- 8 are pending in the case. Specifically, claims 1 and 7 are objected to and claims 1-8 are rejected. Applicant respectfully requests reconsideration of the claim rejections based on the above amendment and following remarks.

Claims 1-8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,426,755 to Yokouchi et al (hereinafter Yokouchi), in view of U.S. Patent No. 6,044,282 to Hlasny (hereinafter Hlasny). The Examiner stated essentially that the combined teachings of Yokouchi and Hlasny teach or suggest all the limitations of the claimed invention.

Amended claim 1 recites, inter alia, a processor clock generation circuit for a low power consumption modem chip design, comprising:

a decoder for decoding an externally inputted instruction to check whether the inputted instruction is a power-down instruction or a power-up instruction, and generating control signals;

a clock selection unit for, if the instruction is the power-down instruction, outputting the second clock signal as a processor clock signal and outputting a clock change end signal in response to a control signal outputted from the decoder and, if the instruction is the power-up instruction, outputting the first clock signal as the processor clock signal in response to the outputted control signal from the decoder and a first clock wake-up end signal; and

a first clock controller for, if the instruction is the power-down instruction, outputting the disable signal for disabling clock generation of the first clock generator in response to the control signal outputted from the decoder and the clock change end signal outputted from the clock selection unit and, if the instruction is the power-up instruction, outputting the enable signal for enabling the clock generation of the first clock generator in response to the control signal

outputted from the decoder, and outputting the first wake-up end signal after a predetermined time.

Yokouchi teaches a semiconductor device including a sense amplifier such that a storage device can be read at a high speed and at a low speed, whereby low power consumption may be realized by low speed reading. However, as stated by the Examiner, Yokouchi does not teach a decoder for decoding external instructions to check whether the instruction is a power-up or power-down instruction and generating control signals accordingly. Nor does Yokouchi teach generating a clock change end and /or a wake-up end signal in response to control signals generated when power-down or power-up instructions are detected respectfully as recited in claim 1.

Hlasny discloses a device for use in a portable communication unit in various timing resolution functions. Hlasny teaches using a low power and low speed oscillator to measure a majority of the inactive period to save battery power. Since a low speed oscillator has a frequency that is too low to provide a resolution necessary for accurate timing, Hlasny uses a high frequency oscillator to time a small portion of the inactive period. Thus, the purpose of Hlasny is to combine a fine resolution of the time segment measured by a high speed oscillator, with segment of time measured by a low speed oscillator, in order to yield a measurement of the inactive period that is approximately the same as obtained by using only the high speed oscillator. Accordingly, the rest interval of the high speed clock disclosed in Hlasny is timed by three predetermined wait time intervals, not by an input power-down instruction as recited in claim 1. Likewise, the enabling of the high speed clock in Hlasny is timed by the first counter circuit finishing counting a first wait time, not by an input power-up instruction as recited in claim 1.

Therefore, Hlasny does not teach nor disclose using a high speed clock or a slow speed clock as a processor clock signal; a high speed clock being disabled by a disable signal output from a high speed clock controller in response to a power-down instruction; nor a high speed clock being enabled by an enable signal output from a high speed clock controller in response to a power-up instruction, essentially as recited in claim 1.

Therefore, even if assuming arguendo, that the teachings of Yokouchi and Hlasny were combinable, the combination does not teach or suggest a first clock controller for outputting a disable signal for disabling clock generation of the first clock generator in response to the control signal outputted from the decoder and the clock change end signal outputted from the clock selection unit when receiving a power-down instruction, and outputting an enable signal for enabling the clock generation of the first clock generator in response to the control signal outputted from the decoder when receiving a power-up instruction, as recited in claim 1.

Therefore, for at least the above reasons, claim 1 is believed to be patentably distinct and patentable over Yokouchi and Hlasny.

Claims 2 to 6 depend from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1.

Claim 7 recites, inter alia, a method for generating a clock signal for a processor having a first clock generator for generating a first clock signal and a second clock generator for generating a second clock signal that is lower, in frequency, than the first clock signal, the method comprising:

decoding an externally inputted instruction to check whether the instruction is a power-down instruction and a power-up instruction;

if the instruction is the power-down instruction, then performing a power down method comprising:

selecting a clock signal supplied to the processor as the second clock signal;

generating a clock change end signal; and

controlling the first clock generator to interrupt generation of the first clock signal, if the instruction is the power-up instruction, then performing a power-up method comprising:

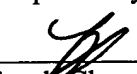
controlling the first clock generator to interrupt generation of the first clock signal;

As discussed above, neither Yokouchi nor Hlasny, separately or combined, teach or suggest a method for "selecting a clock signal supplied to the processor as the second clock signal, generating a clock change end signal, and controlling a first clock generator to interrupt generation of the first clock signal depending on a power-up or power-down instruction," as claimed in claim 7.

Therefore, claim 7 is believed to be patentable over Yokouchi-Hlasny. Claim 8 depends from claim 7 and is believed to be patentable over Yokouchi-Hlasny for at least the same reasons given for claim 7.

For the foregoing reasons, claims 1-8 are believed to be allowable. The Examiner's withdrawal of the claim rejections is respectfully requested. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,



Frank Chau
Reg. No. 34,136
Attorney for Applicant

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury New York 11797
TEL: (516) 692-8888
FAX: (516) 692-8889